The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An electro-optical device of an active matrix comprising:

a gate line provided [[on]] over a substrate;

a data line provided [[on]] over said substrate;

a wiring provided [[on]] over said substrate;

a pixel electrode provided [[on]] over said substrate and superposed on said gate line with an insulator therebetween and superposed on said wiring with an insulator therebetween; and

at least one transistor provided [[on]] over said substrate and connected with said gate line at a gate thereof and connected with said data line at one of source and drain thereof and connected with said pixel electrode at the other one of the source and drain,

wherein a capacitance between said pixel electrode and said gate line and a capacitance between said pixel electrode and said wiring are the same as each other.

2. (Currently Amended) A device according to claim 1 wherein said wiring is another gate line provided [[on]] over said substrate.

3. (Previously Presented) A device according to claim 1 wherein said wiring is in parallel with said gate line.

4. (Canceled)

5. (Currently Amended) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided [[on]] over a substrate;

a gate line of (n+1)-th row provided [[on]] over said substrate;

a gate line of (n+2)-th row provided [[on]] over said substrate;

a data line of m-th column provided [[on]] over said substrate;

a pixel electrode of n-th row and m-th column provided [[on]] over said substrate and connected with said data line and said gate line of n-th row through corresponding at least one transistor; said pixel electrode being superposed on said gate line of (n+1)-th row with an insulator therebetween and superposed on said gate line of n-th row with an insulator therebetween; and

a pixel electrode of (n+1)-th row and m-th column provided [[on]] over said substrate and connected with said data line and said gate line of (n+1)-th row through corresponding at least one transistor, said pixel electrode of (n+1)-th row and m-th column being superposed on said gate line of (n+2)-th row with an insulator therebetween and superposed on said gate line of (n+1)-th row with an insulator therebetween,

wherein said pixel electrode of n-th row and m-th column is provided on an opposite side of said data line to said pixel electrode of (n+1)-th row and m-th column.

6. (Currently Amended) An electro-optical device of an active matrix comprising:

a first gate line provided [[on]] over a substrate;

a first data line provided [[on]] over said substrate;

a second gate line provided [[on]] over said substrate and adjacent to said first gate line;

a second data line provided [[on]] over said substrate and adjacent to said first data line; and

a pixel electrode provided [[on]] over said substrate and connected with said first gate line and said first data line through at least one transistor, a gate thereof being connected with said first gate line and one of source and drain thereof being connected

with said first data line and the other one of the source and drain being connected with said pixel electrode,

wherein said pixel electrode has substantially the same shape of an area surrounded by said first data line and said second data line and said first gate line and said second gate line, and said pixel electrode is enclosed by said first data line and said second data line and said first gate line and said second gate line.

7. (Original) The device of claim 6 wherein said pixel electrode is superposed on said first data line and said second data line and said first gate line and said second gate line to form capacitors, respectively.

8. (Original) The device of claim 7 wherein the capacitor formed by said pixel electrode and said first data line and the capacitor formed by said pixel electrode and said second data line have capacitances smaller than those of the capacitor formed by said pixel electrode and said first gate line and the capacitor formed by said pixel electrode and said second gate line.

9.-20. (Canceled)

21. (Currently Amended) An electro-optical device of an active matrix comprising:

a first pixel electrode formed [[on]] over a first gate line with an insulator therebetween wherein said first gate line is provided [[on]] over a substrate;

a second pixel electrode formed [[on]] over a second gate line with said insulator therebetween, said second pixel electrode being formed adjacent to said first pixel electrode, wherein said second gate line is provided [[on]] over said substrate;

a data line provided [[on]] over said substrate;

an exclusive wiring provided [[on]] over said substrate, said exclusive wiring being formed between said first and second gate lines and being formed under said first pixel electrode with said insulator therebetween; and

at least one transistor provided [[on]] over said substrate and connected with said first gate line at a gate thereof and connected with said data line at one of source and drain thereof and connected with said first pixel electrode at the other one of the source and drain,

wherein a first capacitance between said first pixel electrode and said first gate line and a second capacitance between said first pixel electrode and said exclusive wiring are the same as each other.

22. (Currently Amended) An electro-optical device of an active matrix comprising:

a first gate line provided [[on]] over a substrate;

a second gate line provided adjacent to said first gate line [[on]] over said substrate;

a first pixel electrode provided [[on]] over said substrate and connected with said first gate line through at least one first transistor; and

a second pixel electrode provided [[on]] over said substrate and connected with said second gate line through at least one second transistor,

wherein said first pixel electrode is superposed on said first gate line with an insulator therebetween and is superposed on said second gate line with another insulator therebetween, and

wherein a difference between area shared by said first gate line and said first pixel electrode and area shared by said second gate line and said first pixel electrode is not more than one tenth of sum of said area shared by said first gate line and said first pixel electrode and said area shared by said second gate line and said first pixel electrode.

23. (Canceled)

24. (Currently Amended) An electro-optical device of an active matrix comprising:

a gate line provided [[on]] over a substrate;

a data line provided [[on]] over said substrate;

a wiring provided [[on]] over said substrate;

a pixel electrode provided [[on]] over said substrate and superposed on said gate line with an insulator therebetween and superposed on said wiring with an insulator therebetween; and

at least one transistor provided [[on]] over said substrate and connected with said gate line at a gate thereof and connected with said data line at one of source and drain thereof and connected with said pixel electrode at the other one of the source and drain,

wherein a capacitance between said pixel electrode and said gate line and a capacitance between said pixel electrode and said wiring are the same as each other intentionally.

25. (Currently Amended) An electro-optical device of an active matrix comprising:

a gate line provided [[on]] over a substrate;

a data line provided [[on]] over said substrate;

a wiring provided [[on]] over said substrate;

a pixel electrode provided [[on]] over said substrate and superposed on said gate line with an insulator therebetween to form a first capacitance and superposed on said wiring with an insulator therebetween to form a second capacitance;

a first means for applying a first signal to said gate line;

a second means for applying a second signal to said wiring, said second signal having an opposite polarity to said first signal; and

at least one transistor provided [[on]] over said substrate and connected with said gate line at a gate thereof and connected with said data line at one of source and drain thereof and connected with said pixel electrode at the other one of the source and drain.

26. (Previously Presented) A device according to claim 25 wherein said second signal applied to said wiring have the same magnitude of voltage as said first signal applied to said gate line.

27. (Previously Presented) A method according to claim 25 wherein said second signal is synchronized with said first signal.